PARAMETRIC FREQUENCY MULTIPLICATION AND LEVEL CONTROL IN BROADBAND MICROWAVE SIGNAL SOURCE

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Abstract

A frequency multiplier, formed from a step recovery diode and coupled to a YIG filter, is utilized to multiply a synthesized 2—6.2 GHz incoming signal by factors of 1, 2, and 3 while simultaneously filtering the selected harmonic to generate a 2—18.6 GHz output.

Introduction

While tuned multiplier design is now common practice, certain constraints have generally limited their use to narrow band applications where input power to the multiplier is precisely controlled. In particular, a single performance characteristic, wide dynamic operating power range, has restricted the use of this element in broadband, leveled, amplitude modulated signal sources. A discussion on optimizing the design of the multiplier to operate over a greater than 30 dB dynamic range is presented.

Next, the multiplier is considered as an element in the RF forward path of an ALC loop which is capable of regulating power variations to less than ± 1 dB over a 23 dB calibrated power range from 2—18 GHz. Factors such as forward path nonlinearities, detector linearization, system linearization, system compensation, amplitude modulation performance and methods of programmability are considered in the discussion.

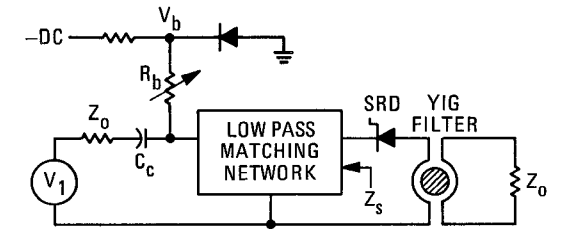
The YIG Tuned Step Recovery Diode Multiplier

The 2—18 GHz output frequencies in the synthesizer are derived from the 2—6 GHz (BAND 1) fundamental synthesized source by passing the signal through the YIG tuned multiplier. In the first band (2—6 GHz), the multiplier is shut off to serve only as a YIG tuned filter. In band 2 (6—12 GHz) and band 3 (12—18 GHz), the multiplier provides rich 2nd and 3rd harmonics of the fundamental input frequencies into the YIG filter, which is magnetically tuned to the desired harmonics rejecting undesirable harmonics and noise.

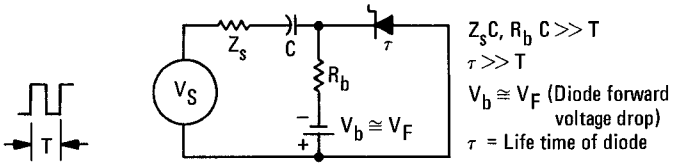
The system design required that, in order to utilize all the available output power the multiplier can deliver, the ALC/AM modulator should be placed before the multiplier and power amplifier (see Fig. D). The output level of the multiplier should thus be capable of being controlled in excess of 30 dB without introducing serious adverse effects on ALC gain or AM performance. Excessive conversion loss variations with input level should be avoided since this will affect the ALC loop stability and AM distortion. The output phase variation with input level variation also should be minimized to satisfy AM to PM conversion requirements.

To achieve the above requirements for the multiplier, an optimum self biasing scheme is applied based on a simplistic approach; keep the conduction angle of the step recovery diode (SRD) constant with regard to input level variation. Using an equivalent circuit of Fig. A at fundamental frequencies with a square wave voltage, the analysis shows that the conduction angle is maintained regardless of input level if the simple bias circuit in Fig. A is incorporated with the multiplier. The results also indicate that the bias resistor value should increase with input frequencies due to decreasing rectification efficiency of the diode. Since the optimum conduction angle may vary between doubler and tripler operation, the optimum resistor values may be chosen differently depending on the bands even at the same input frequency (Fig. B).

These results have been successfully applied to the YIG tuned multiplier. For simplicity, the bias resistor is determined to give maximum power at the high end of the 2nd band and the bias voltage is adjusted to give maximum efficiency at the lowest output power setting. The bias voltage should be approximately a forward voltage drop of a silicon diode. A typical maximum output power over 2—18 GHz is shown in Fig. C.



a. YIG Tuned Multiplier Equivalent Circuit



b. Model For SRD Bias Calculation

Figure A. Step Recovery Diode Bias Model

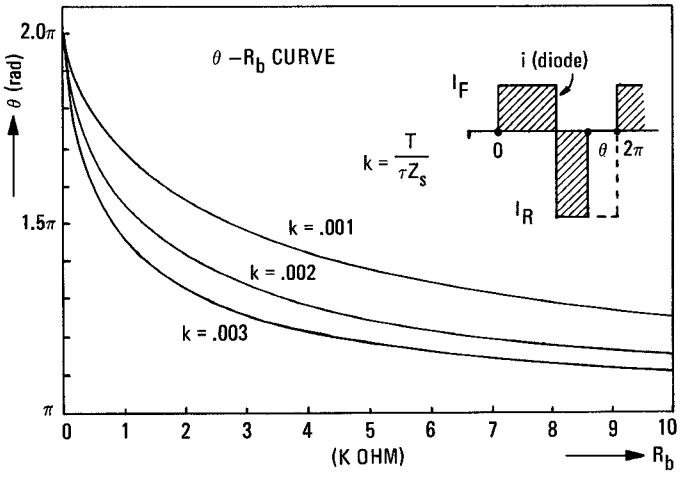


Figure B. Conduction Angle Vs. Bias Resistance (analytically obtained from the model of Fig. A-b)

The input to the multiplier is approximately 20 dBm (100mW) and the output includes loss of 1—2 dB due to a directional coupler, output attenuator, cables, etc. The AM bandwidth is determined by the system bandwidth, however, a significant increase in incidental PM was observed at higher rates. It is believed that the bias circuit time constant becomes too long to rapidly adjust itself for constant conduction angle in the multiplier, thereby increasing phase modulation at the multiplied frequency.

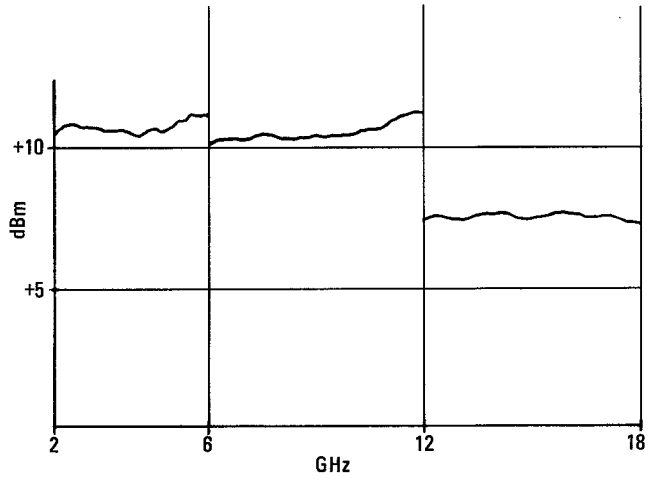


Figure C. Maximum Output Power of 2—18 GHz Synthesizer

2—18 GHz Level Control with Amplitude Modulation

The synthesized source generates the base 2—6.2 GHz signal. A YIG tuned voltage controlled oscillator is the fundametnal source and in conjunction with three additional lock loops, any frequency in the band is generated to step sizes as small as 1 kHz. Components which follow the source must not degrade the phase noise, spectral purity, or switching characteristics beyond established design and theoretical limits. Single sideband phase noise is maintained at —79 dBc in a 1 Hz bandwidth at a 10 kHz offset from the carrier and the broadband noise floor is below —130 dBc thru 18 GHz. Spurious nonharmonically related signals are below —60 dBc while switching time is maintained at less than 15 ms.

A reference voltage, V_{REF}, is established at the intput to the ALC system (Figure D). Generally, an ALC loop is designed such that the reference voltage is directly proportional to V_{out}. However, in the loop to be considered, the reference voltage is proportional to the power output expressed in decibels. The analog method of synthesizing this function is developed by the detector compensation logarithmic amplifier in conjunction with the detector diode characteristics. These elements generate the transfer function

$$V'_{DET} = K\log_{10} V_{OUT}.$$

Substituting

$$V_{OUT} = \sqrt{(P_{OUT}R)}$$

Yields

$$V'_{DET} = \frac{K}{2}\log_{10} P_{out} + \log_{10} R$$

$$= K' P(dbm) + C$$

Thus, by proper selection of K' and C, the detector voltage is linear with power (expressed in decibels). Figure E is the actual measured output voltage of the compensated detector as a function of output power from the source.

The forward gain of the ALC loop is influenced by the following factors:

- Multiplication efficiency as a function of N, frequency, and power input.
- Power variations at the input to the pin diode modulator.
- Modulator transfer function variations.
- Power amplifier gain variations.
- YIG filter passband variations and tuning.
- Directional coupler coupling coefficient variations.
- Detector diode frequency response.

The major forward gain variable is the YIG tuned multiplier while the other factors listed are less significant. To maintain loop stability, while providing the gain necessary for DC level control and high rate AM, requires that the G_2G_{RF} product remain essentially constant. As a result, G_2 is precisely controlled to ensure optimum operating performance with all major variables taken into consideration. To demonstrate the effectiveness of this method, the system is amplitude modulated at a 10 kHz rate to produce 90% AM for various output power settings in each frequency band (N = 1, 2, or 3). The measured results are shown in Figure F. The response depicted, indicates that the operating dynamic range of the system is greater than 30 dB. Note that the applied modulation signal is logarithmically shaped to compensate for detector log compensation.

The compensation voltage, V_{comp}, is generated to remove errors induced by the directional coupler, detector, attenuator, and cables. The variation exhibited graphically in Figure E is a prime example of an

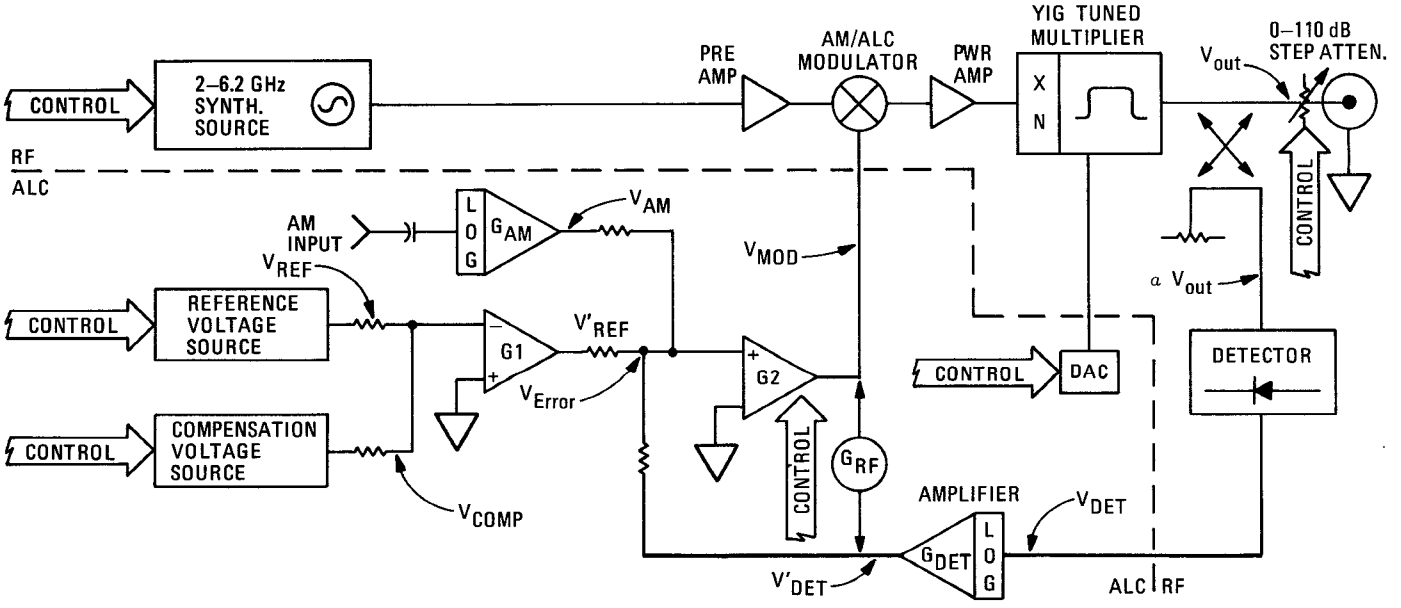


Figure D. The 2—18 GHz ALC System

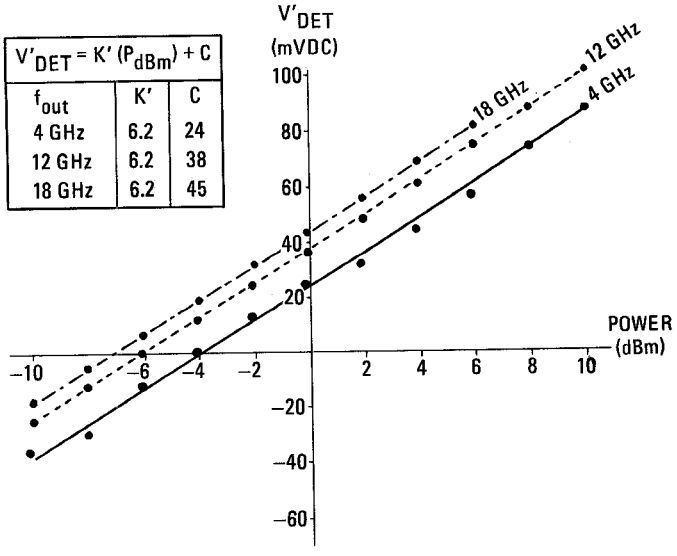


Figure E. Compensated Detector Transfer Characteristics

error which must be corrected. Without compensation, output power variations may exceed 6 dB; but, with compensation, the variation is maintained at less than ± 0.5 dB from 2—18 GHz (Figure G).

Summary

Design considerations for developing a YIG tuned step recovery diode frequency multiplier which operated over 2—18 GHz with a greater than 30 dB dynamic range have been presented. The multiplier was then considered as part of an ALC system where actual performance data was presented. The system discussed is presently utilized in the Hewlett-Packard 8672A Synthesized Signal Generator.

Acknowledgements

Robert Joly was responsible for the initial multiplier design. Roger Stancliff, Ganesh Basawaoatna, Alejandro Chu, Paul Hernday, and Val Peterson provided valuable support to achieve the level of performance realized. ALC developments were supplied by Steve Sparks.

References

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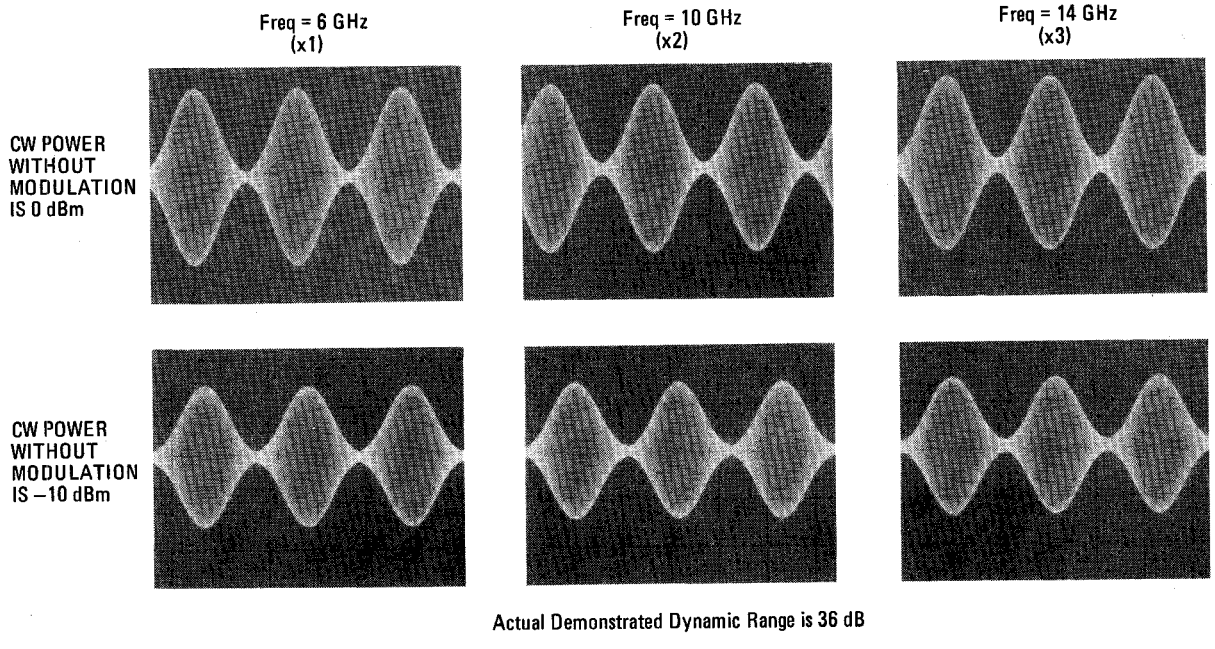

Figure F. Amplitude Modulation as a Function of Frequency and Power

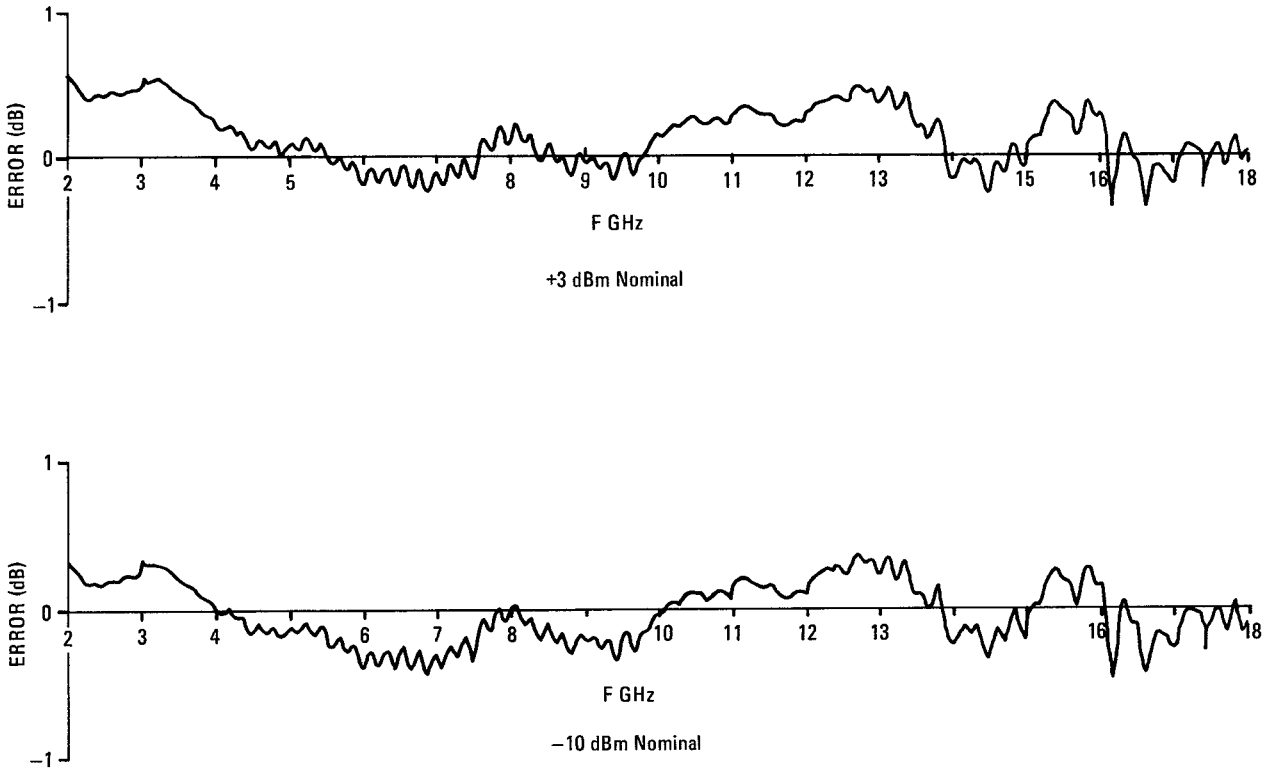

Figure G. Power Flatness Vs. Frequency